

FIG. 1

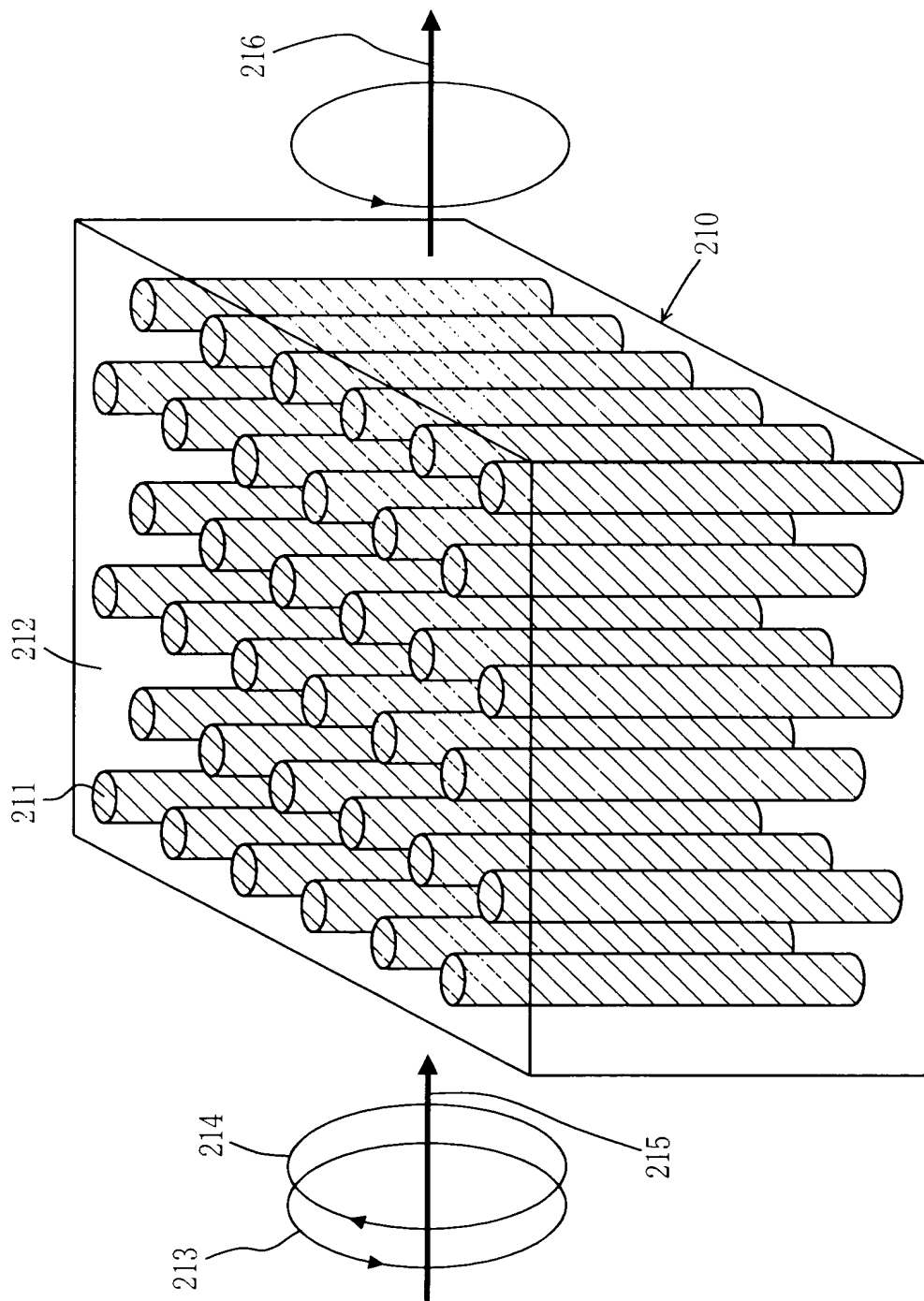
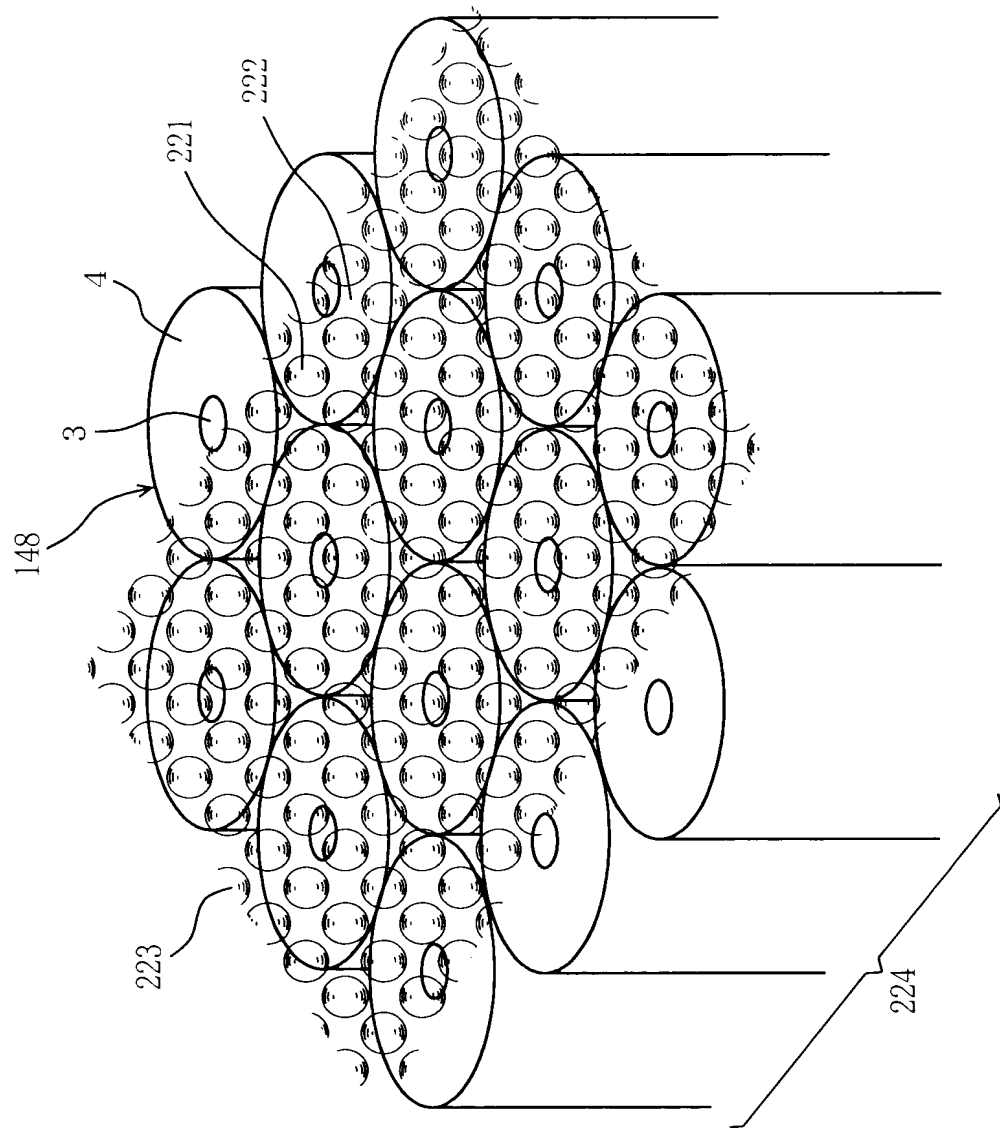


FIG. 2



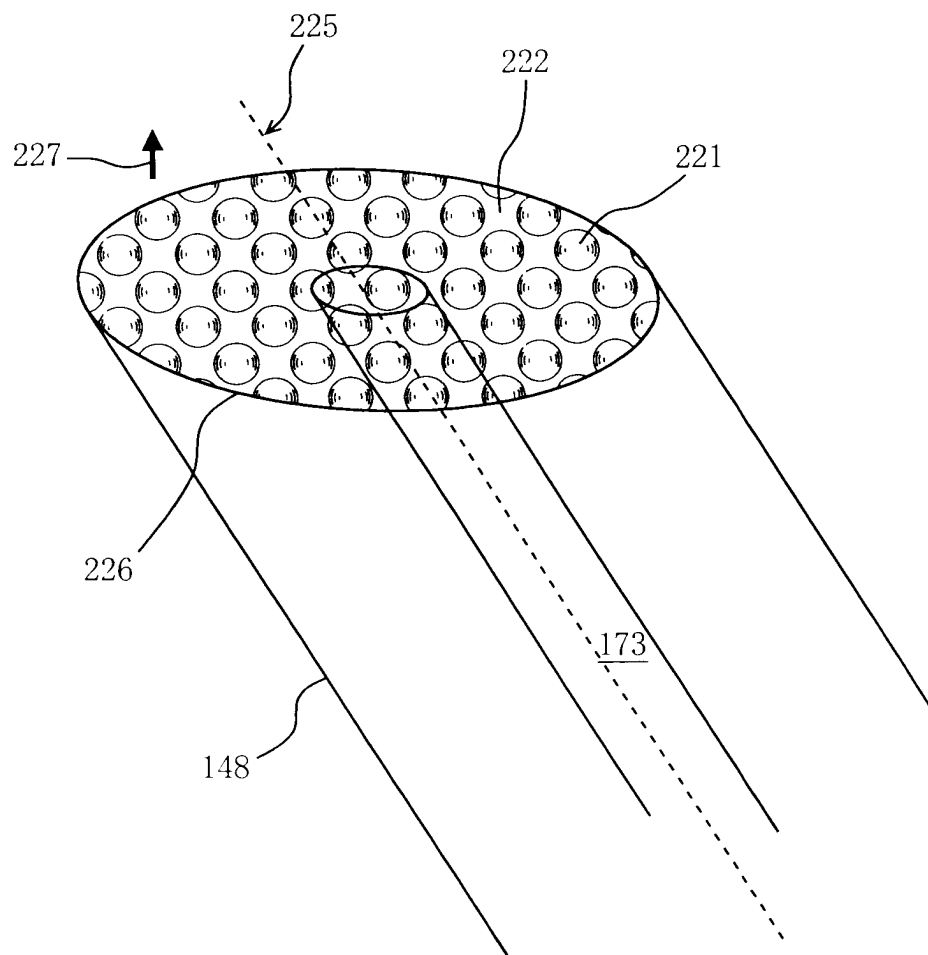
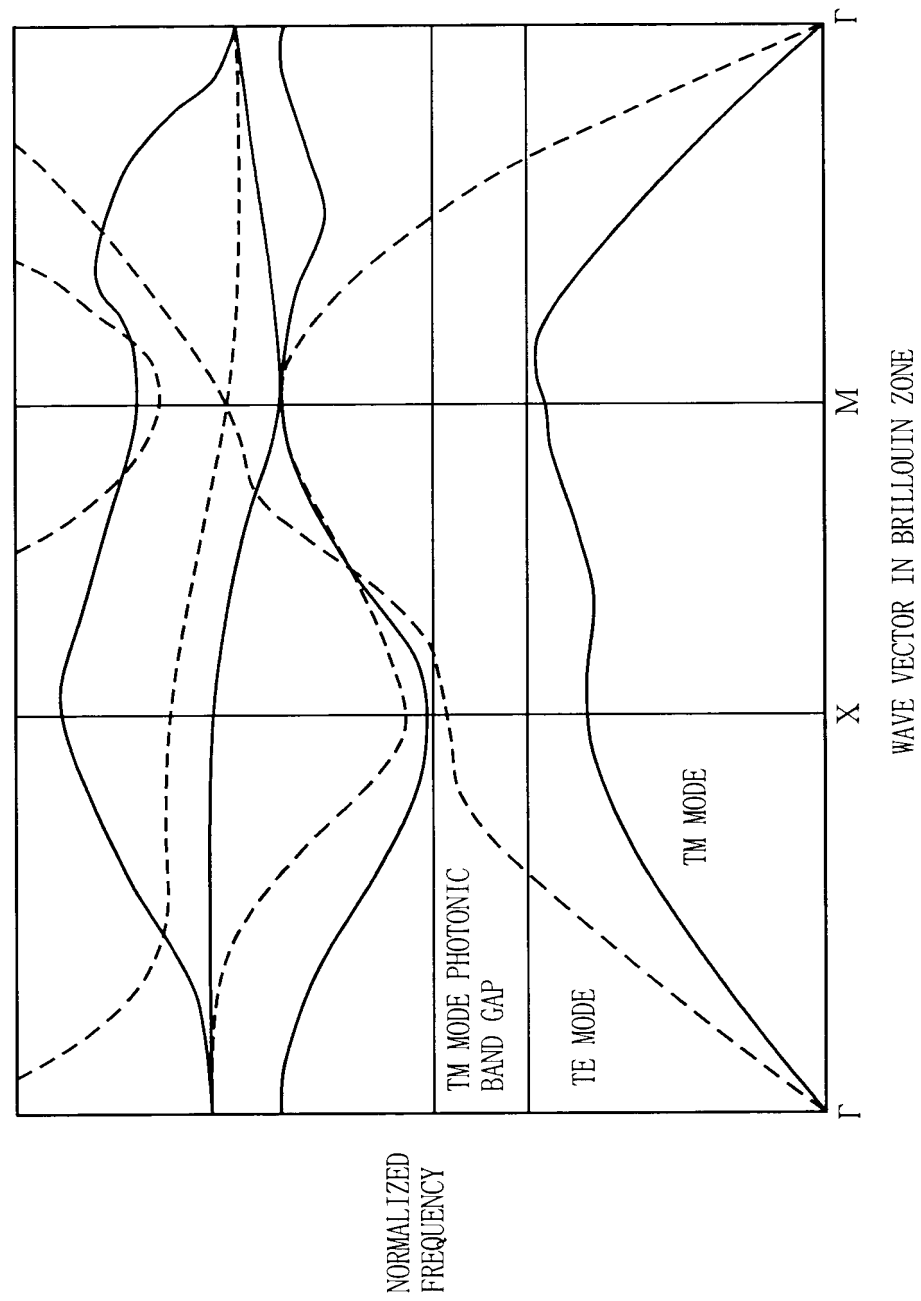


FIG. 4



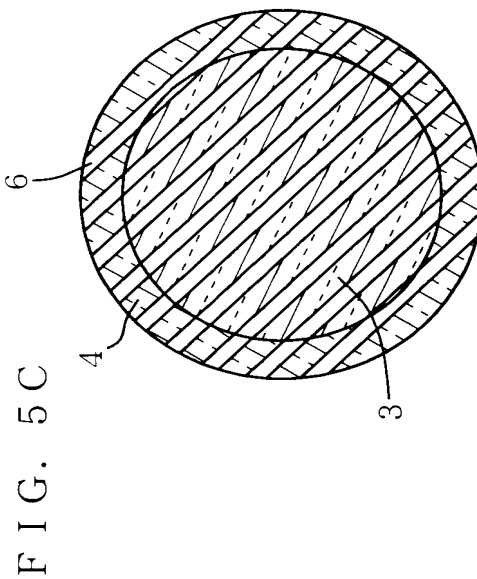
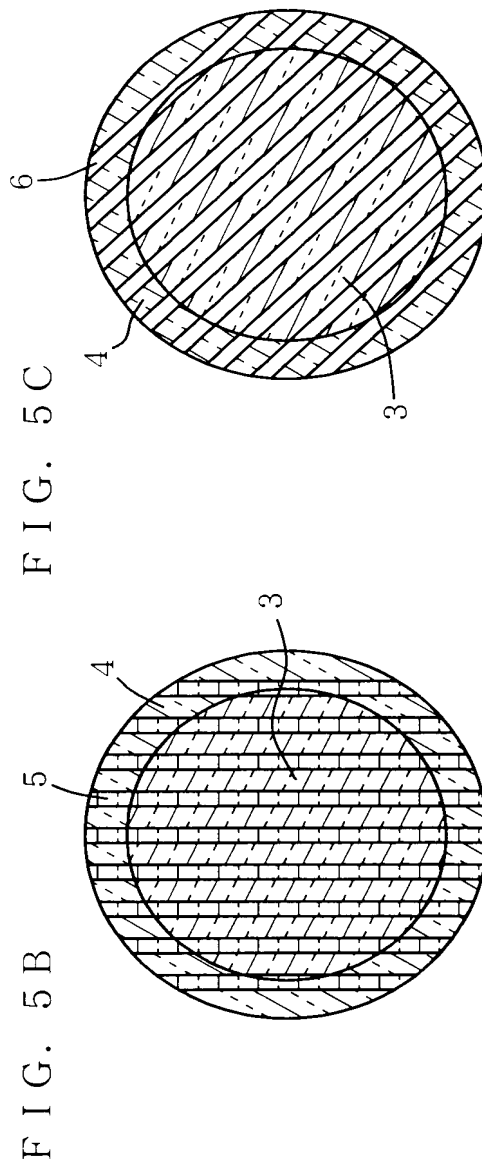
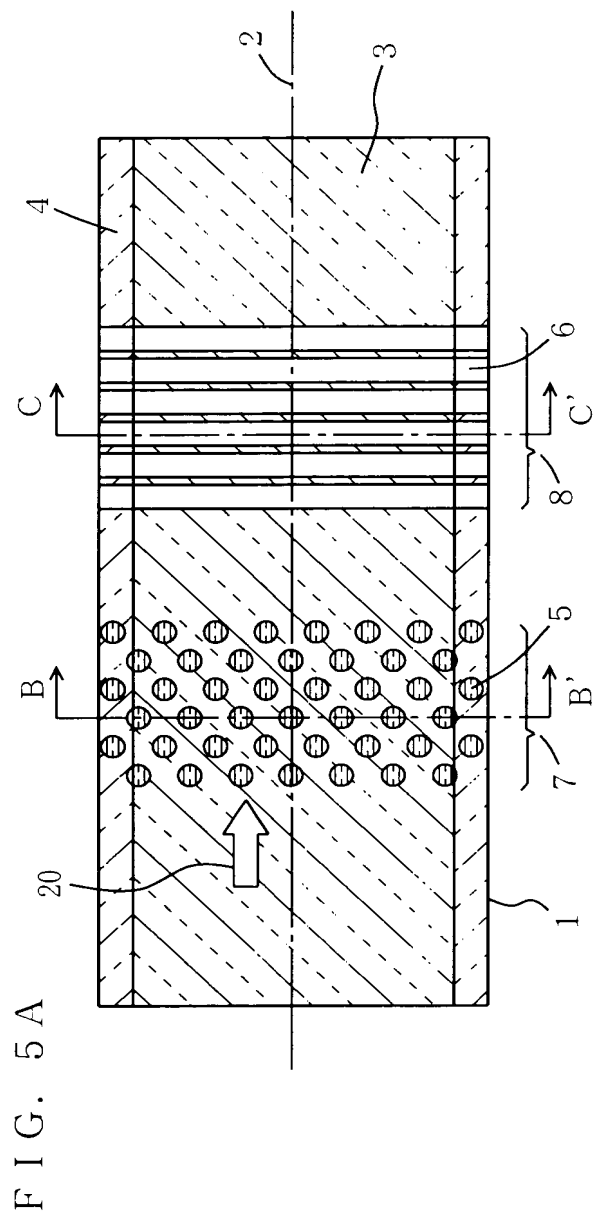


FIG. 6

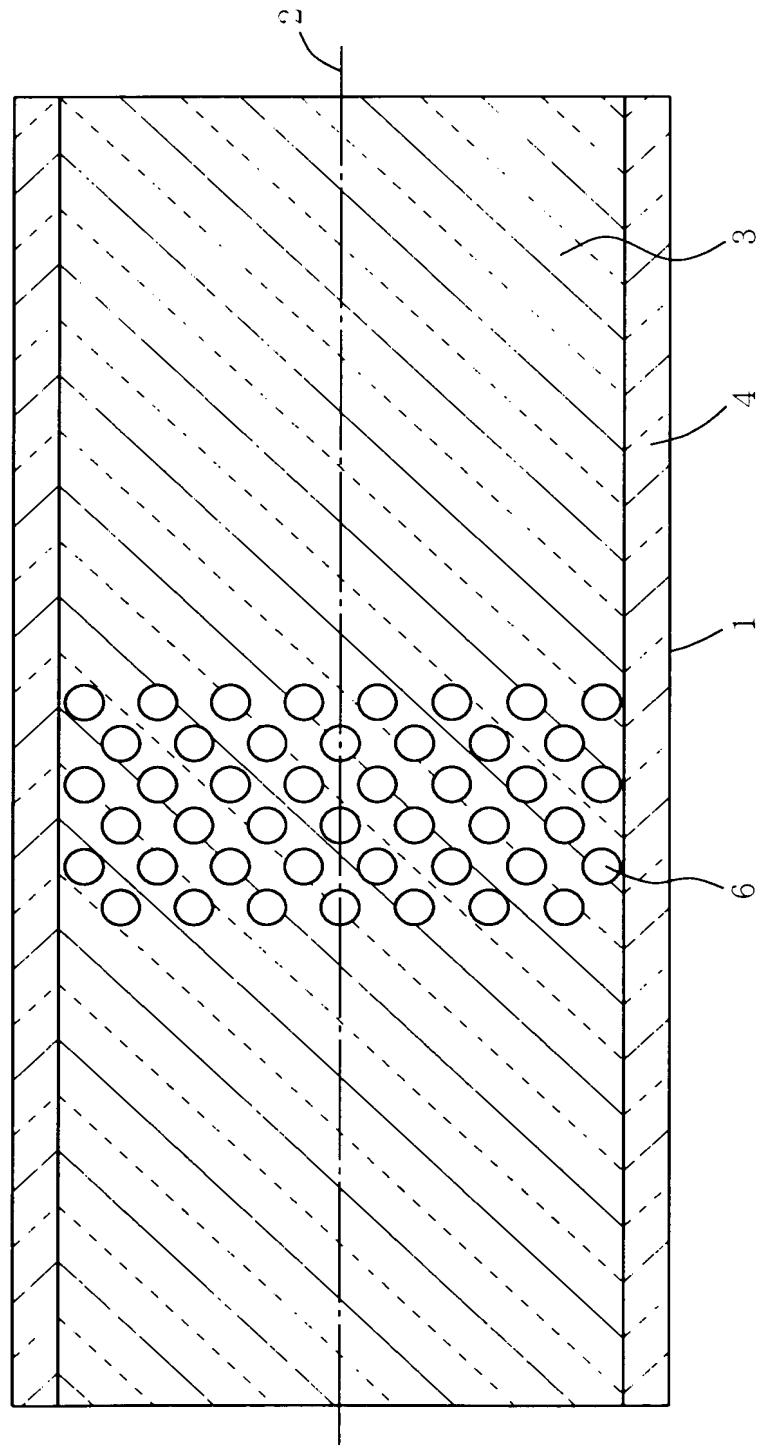


FIG. 7A

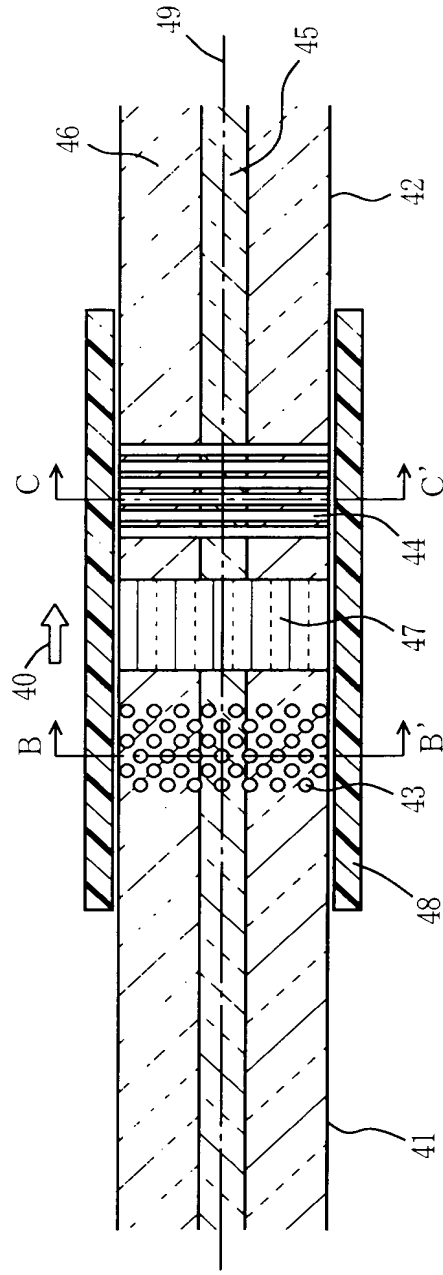


FIG. 7B

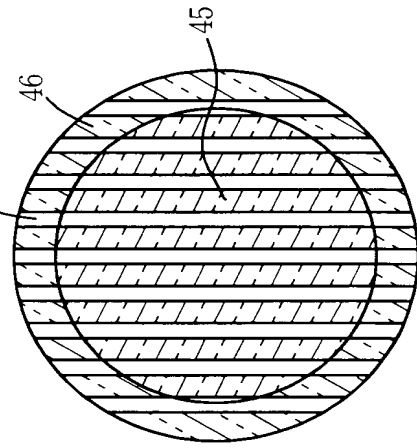


FIG. 7C

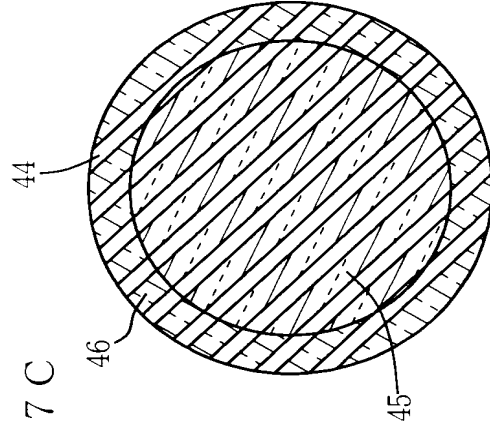


FIG. 8

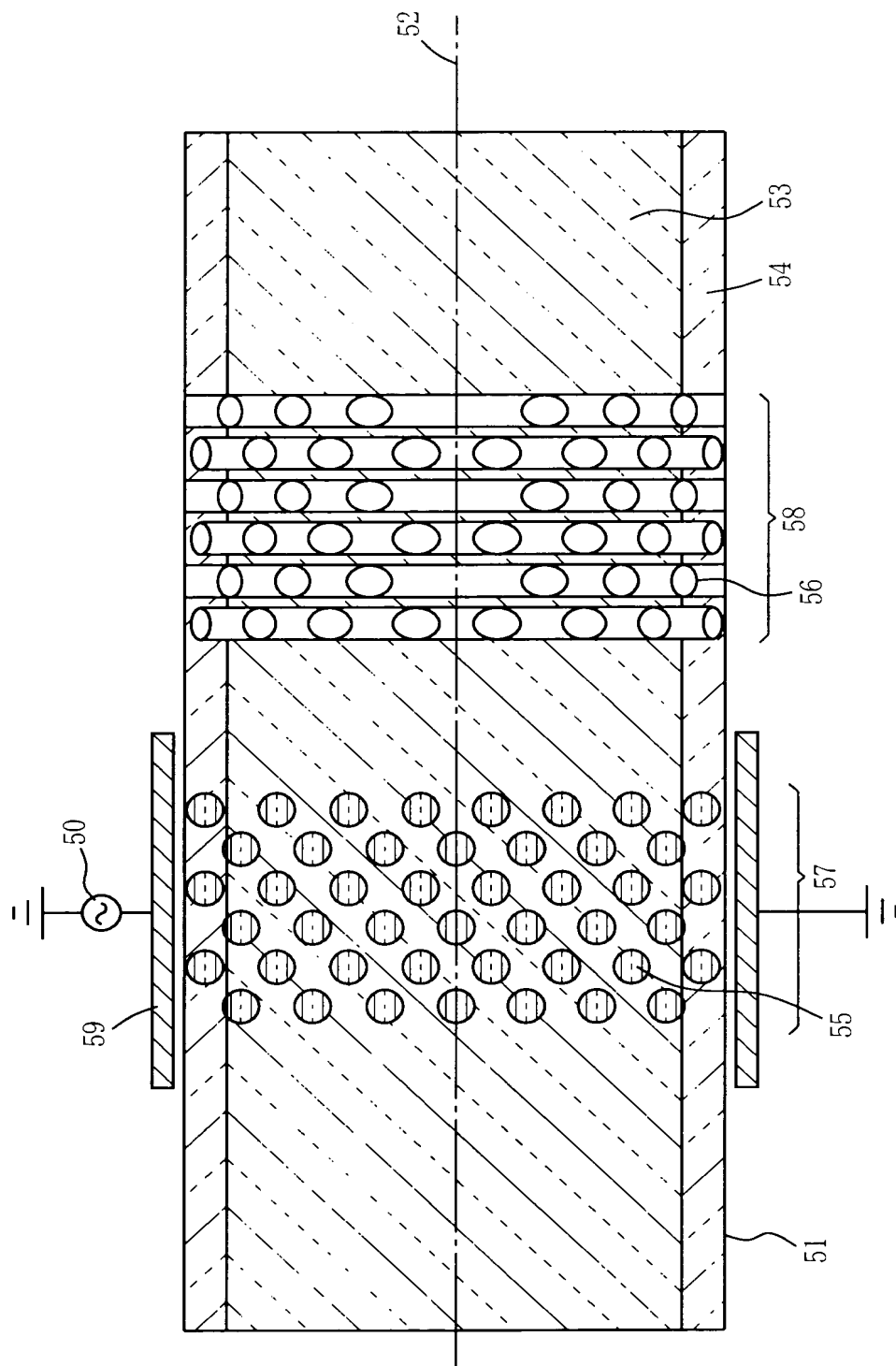




FIG. 9

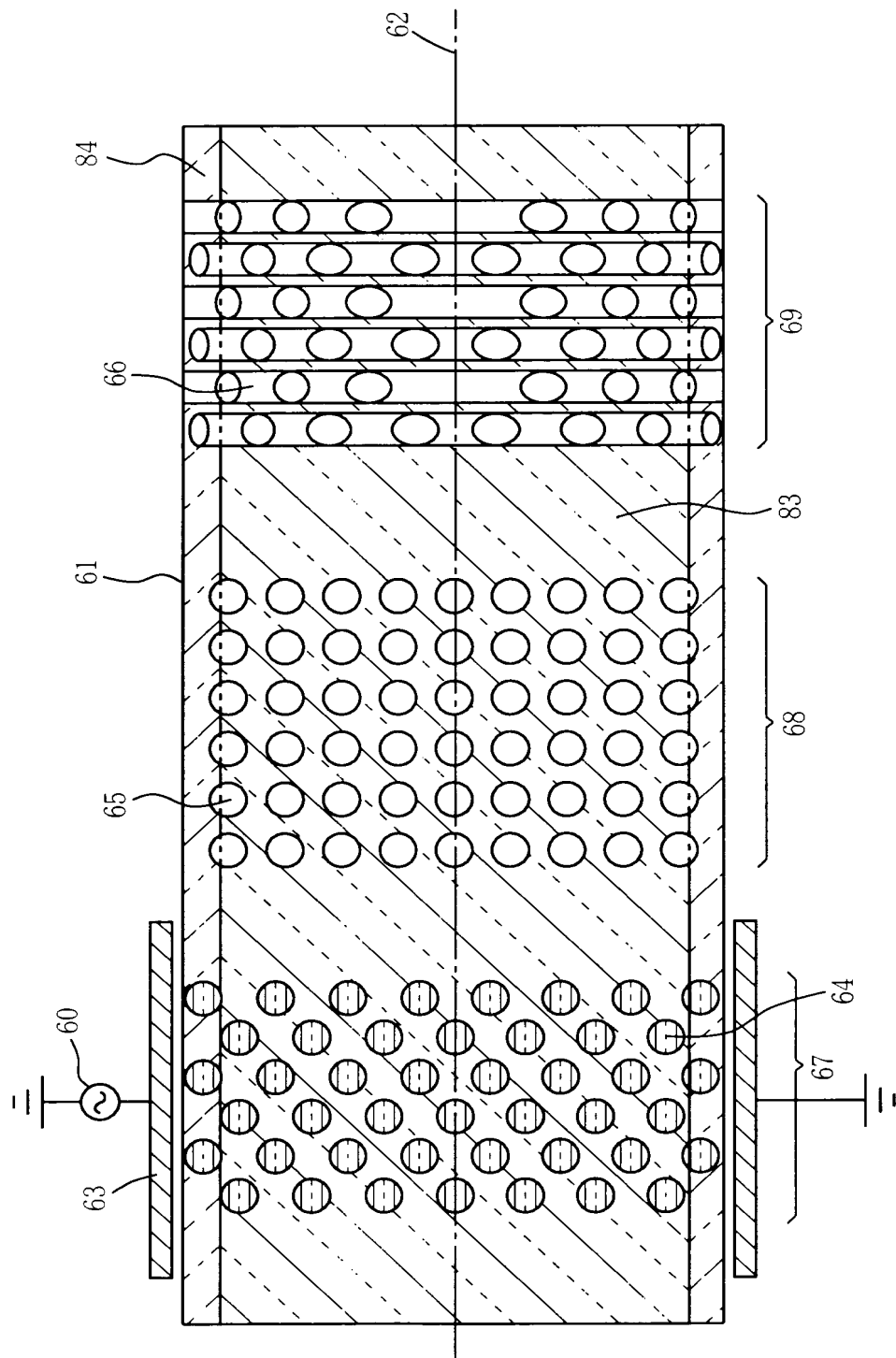


FIG. 10

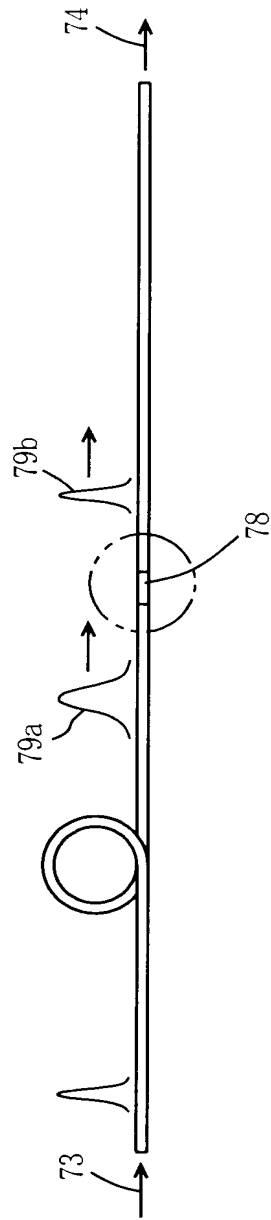


FIG. 11

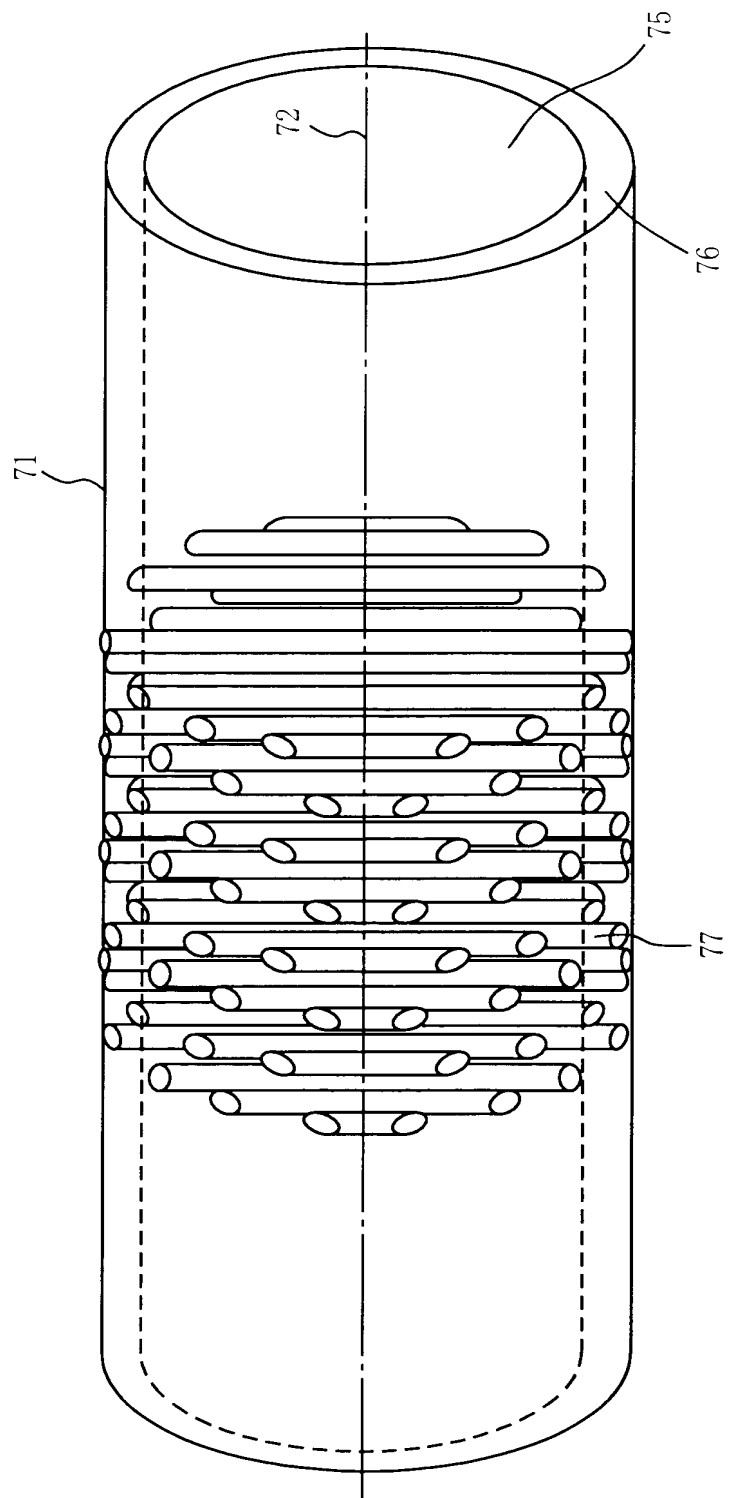


FIG. 12

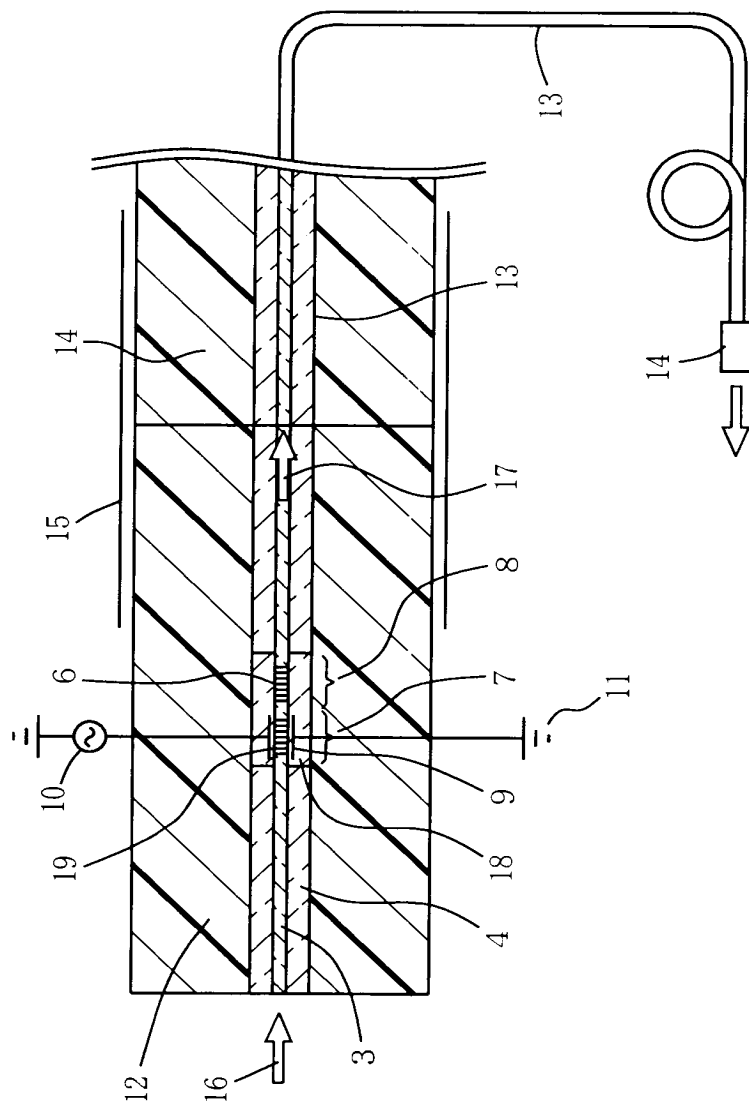


FIG. 13B

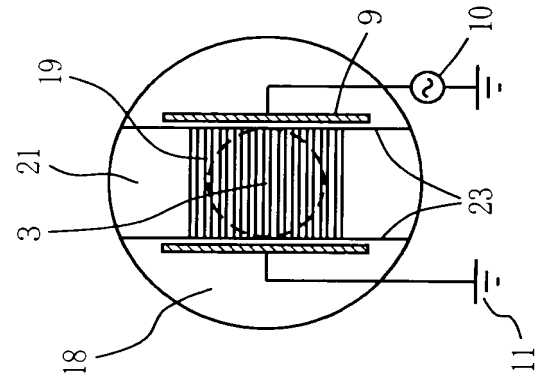


FIG. 13A

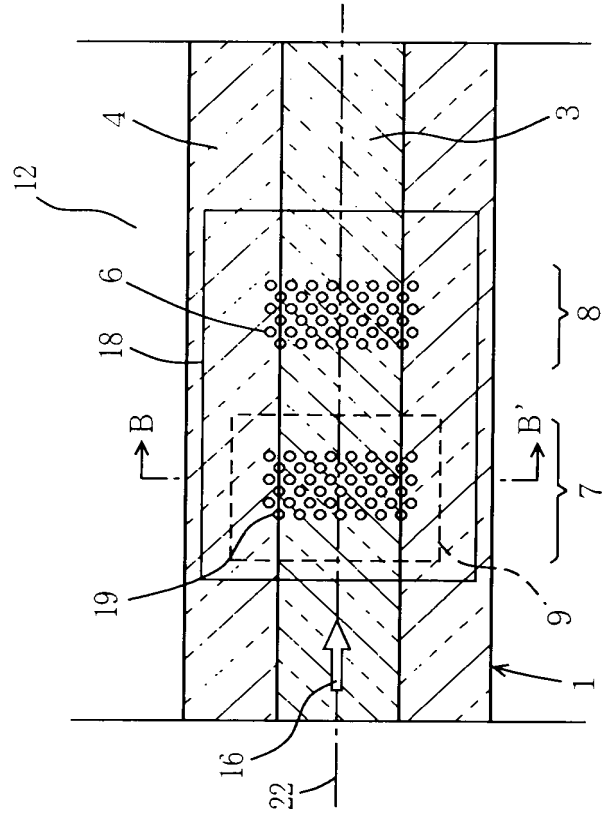


FIG. 14B

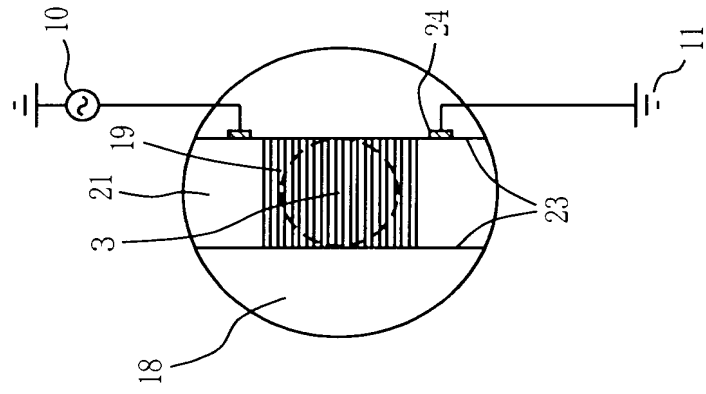


FIG. 14A

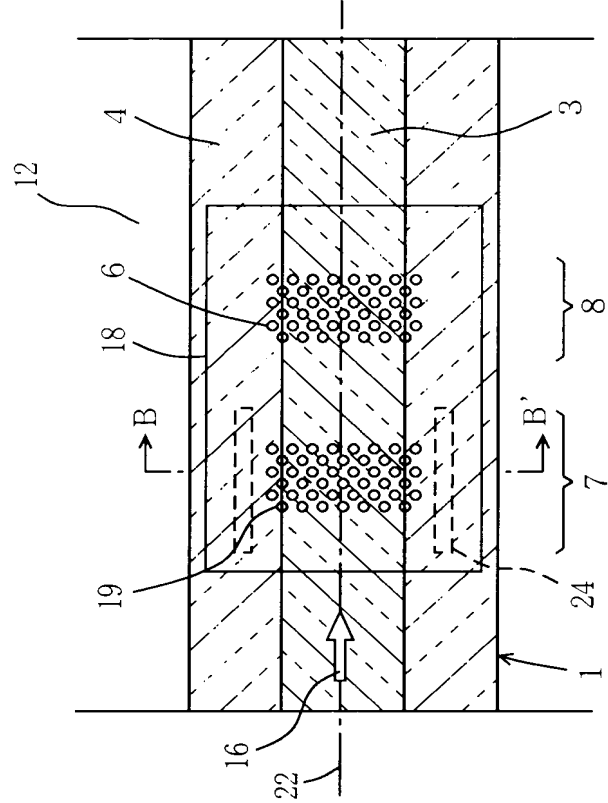




FIG. 16B

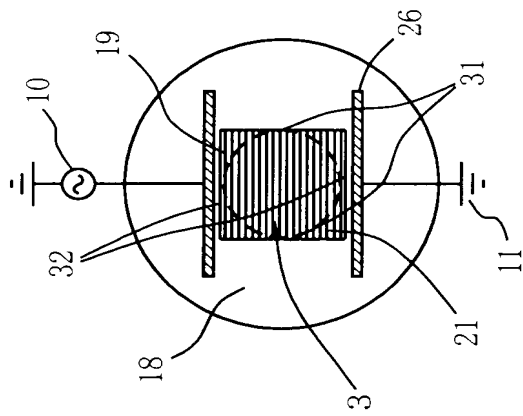


FIG. 16A

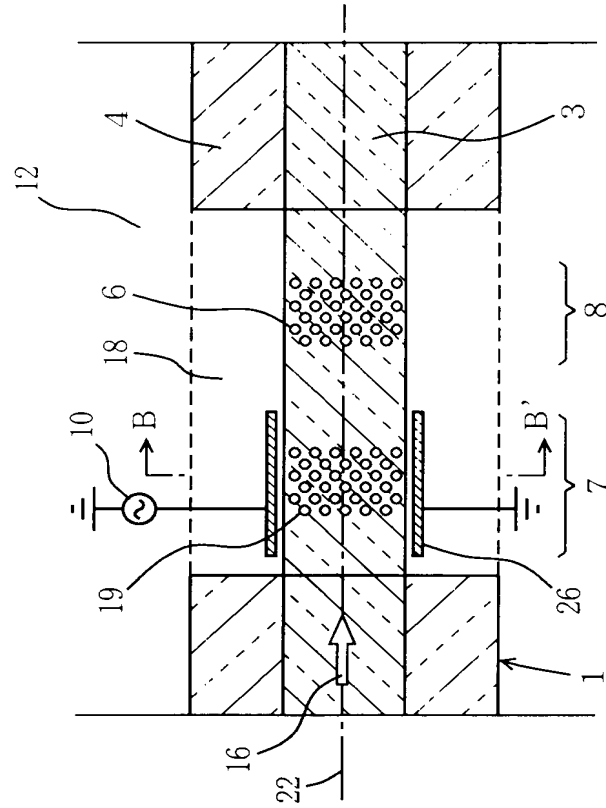






FIG. 18A

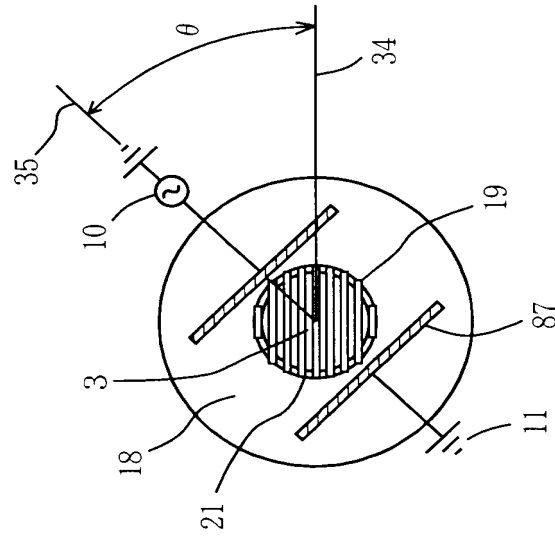


FIG. 18B

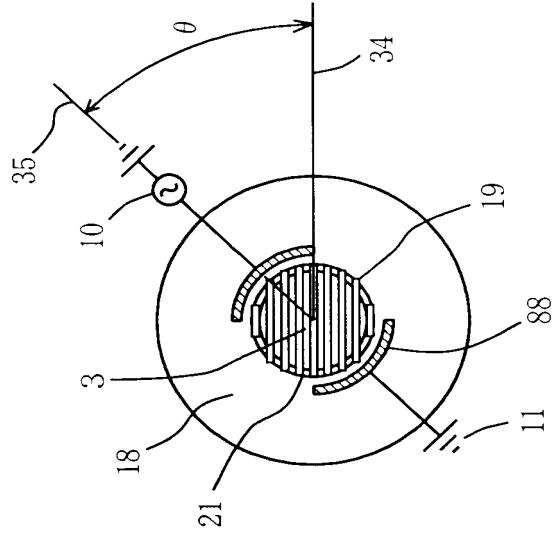


FIG. 19

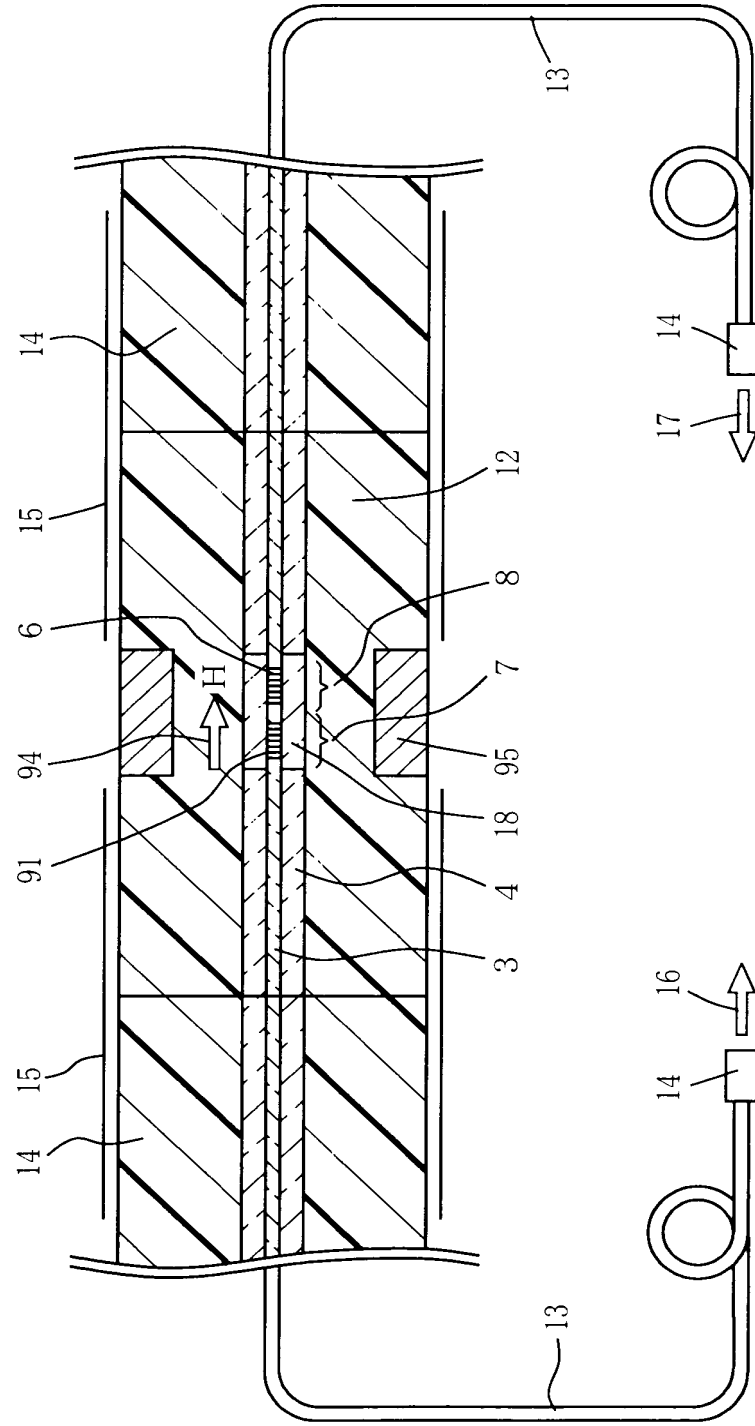


FIG. 20

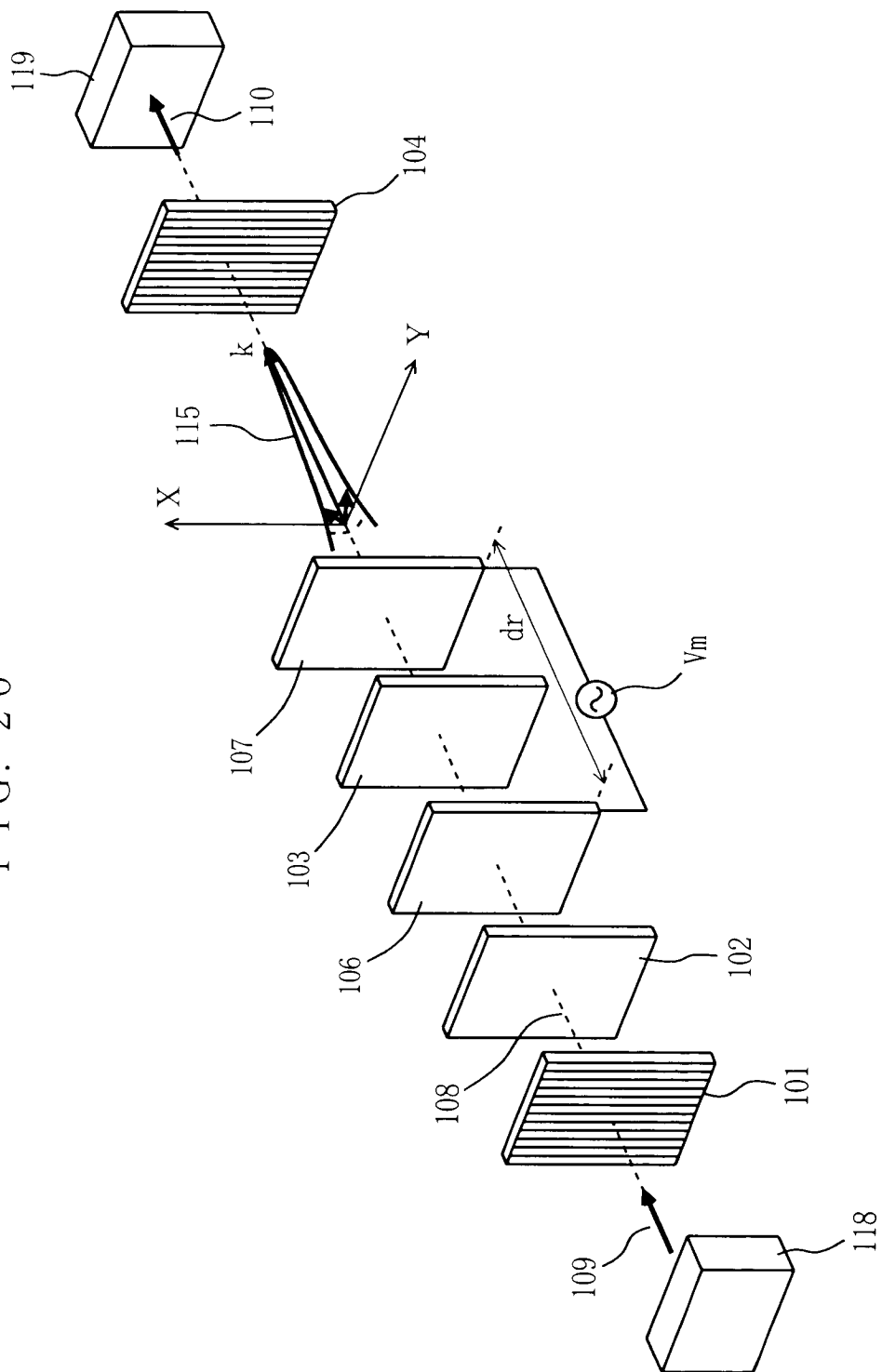
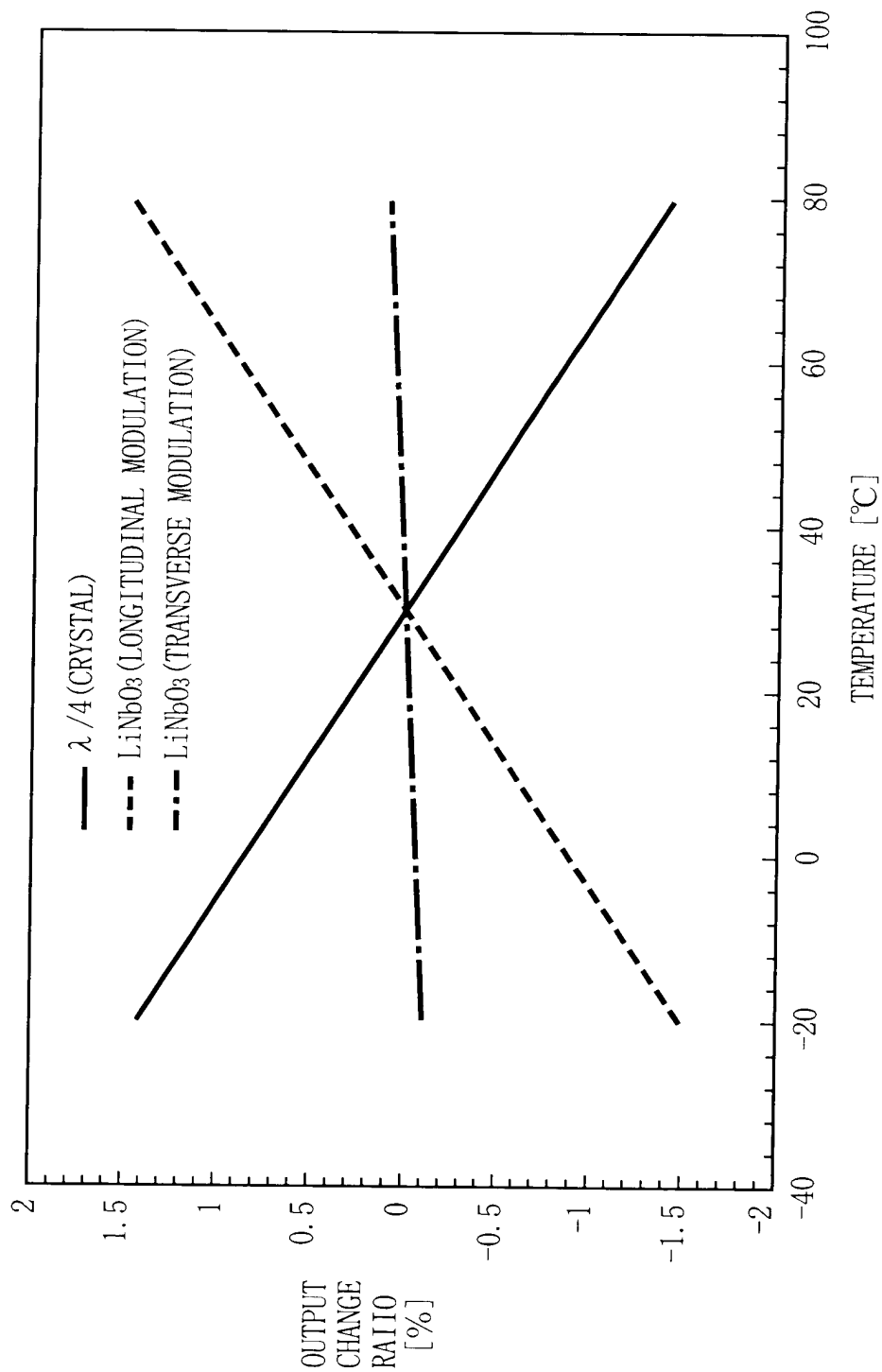


FIG. 21



F I G . 2 2

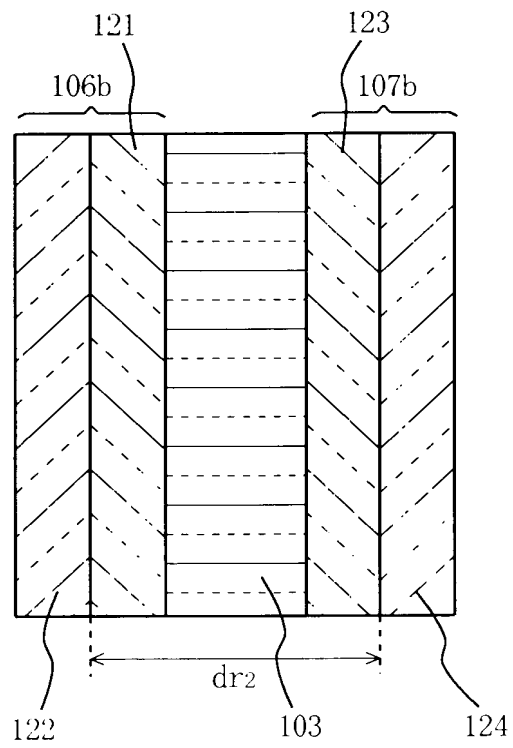


FIG. 23

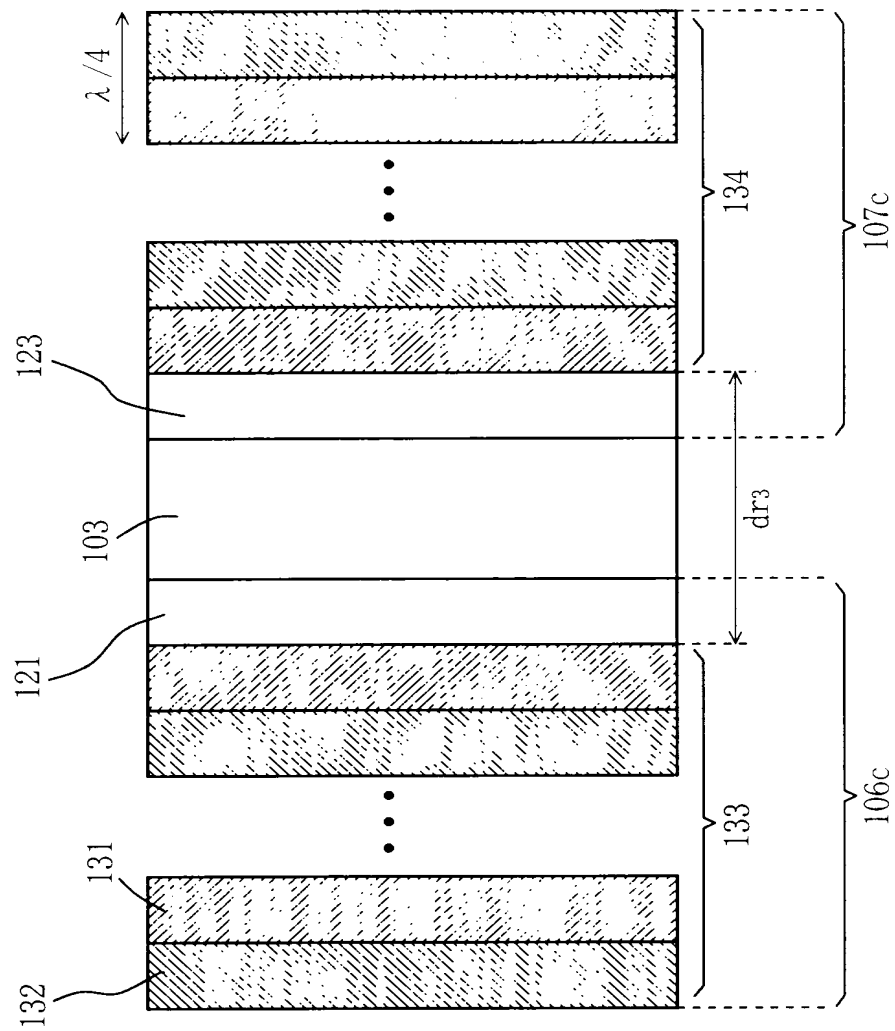


FIG. 24

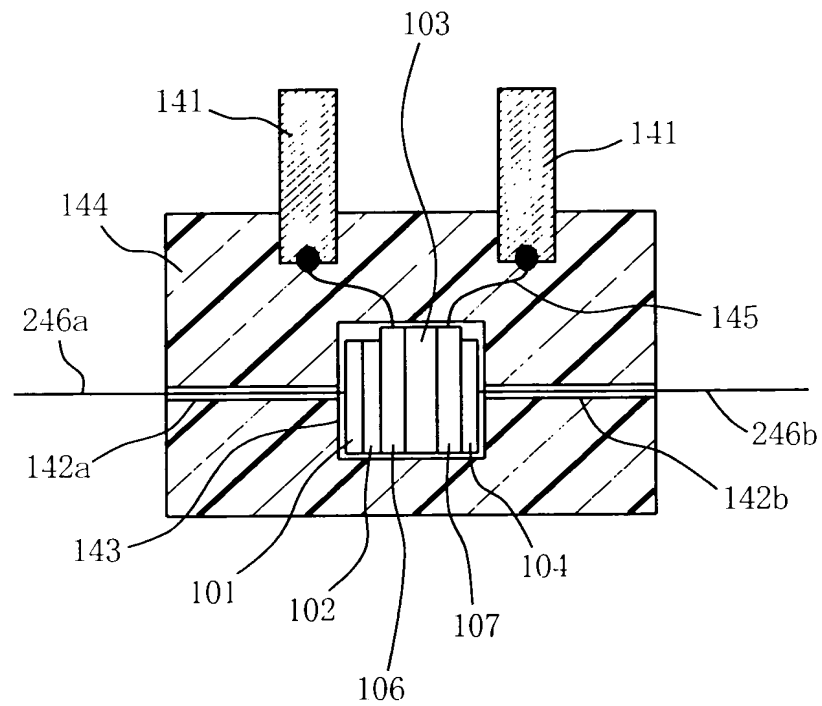
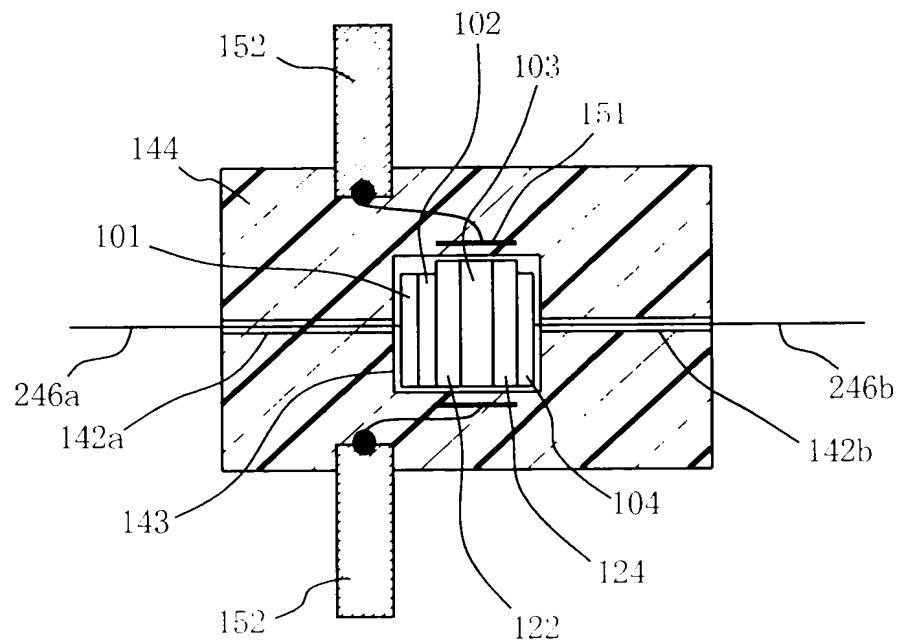


FIG. 25





A cross-sectional view of a semiconductor device. The device features a central channel region 102 flanked by source/drain regions 106 and 107. The channel region 102 contains a gate stack 103, which includes a layer 145 and a layer 148a. The source/drain regions 106 and 107 contain a gate stack 144, which includes a layer 148b and a layer 142a/b. A contact layer 171 is shown at the bottom of the device.

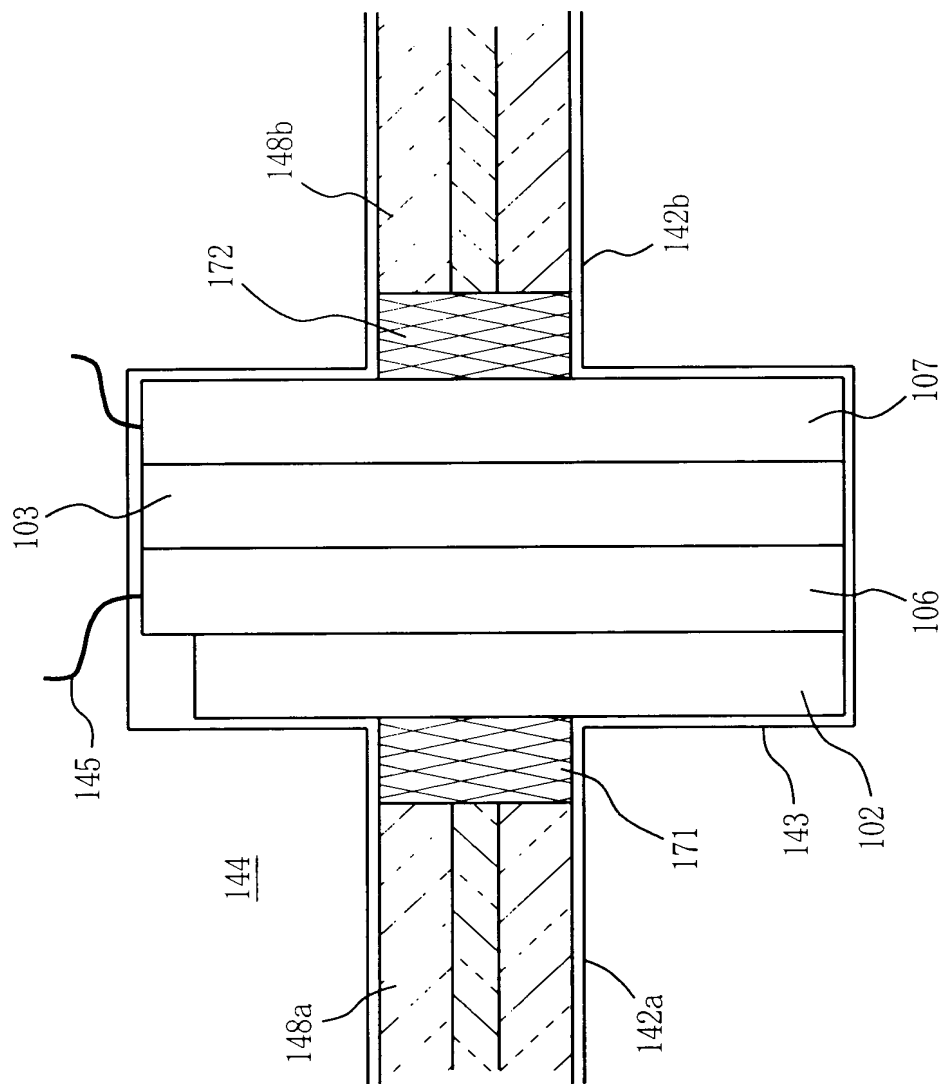


FIG. 27

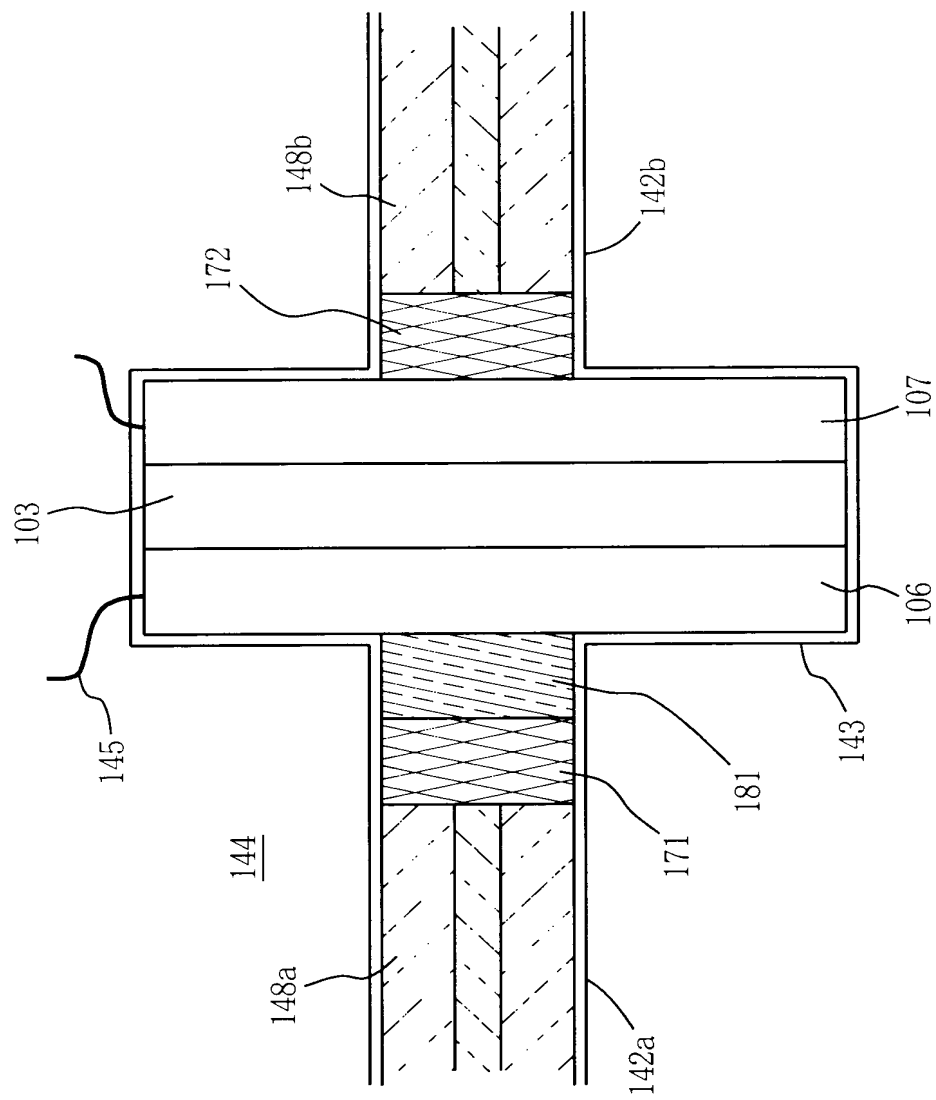


FIG. 28

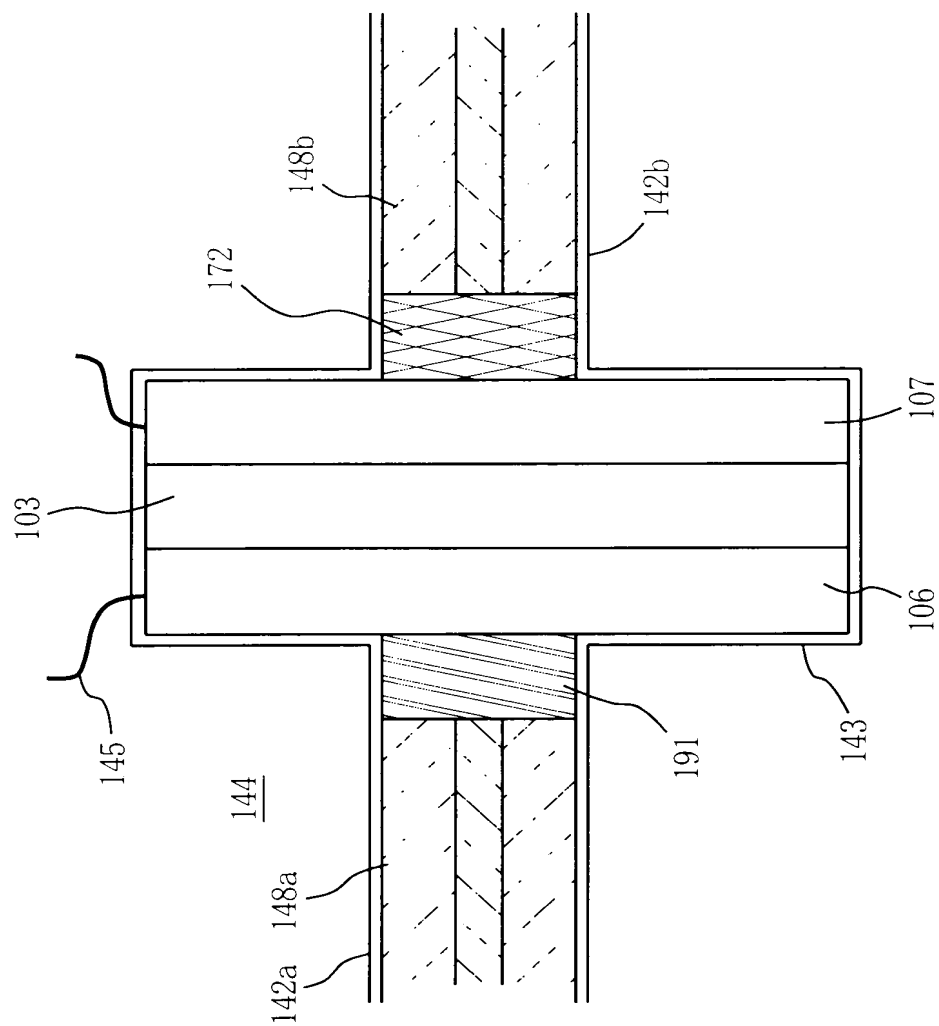
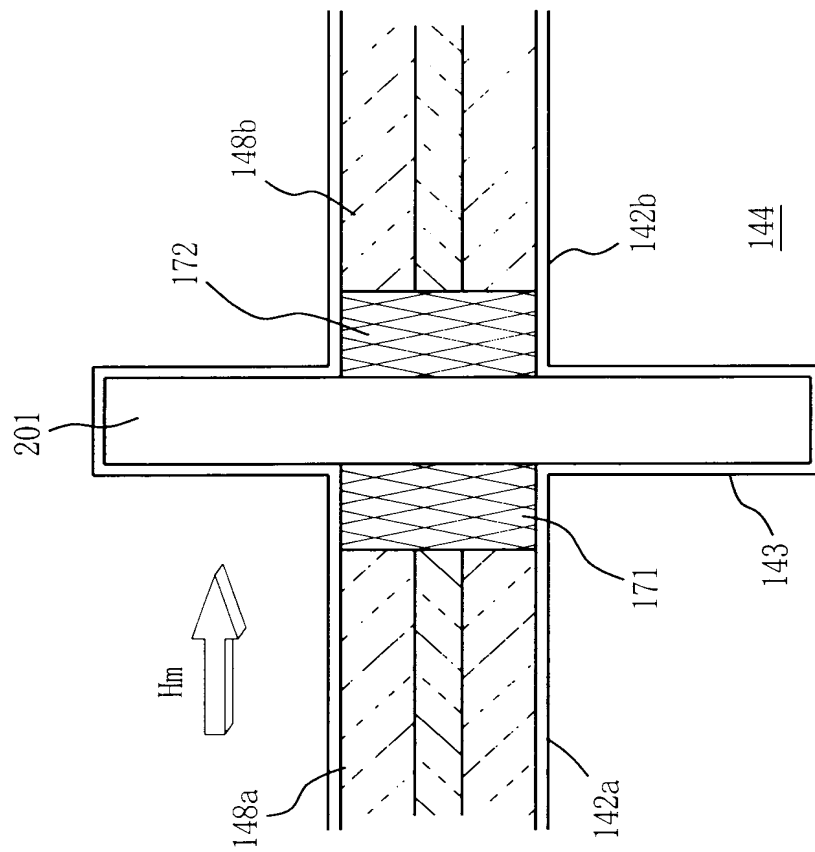


FIG. 29



F I G. 3 0

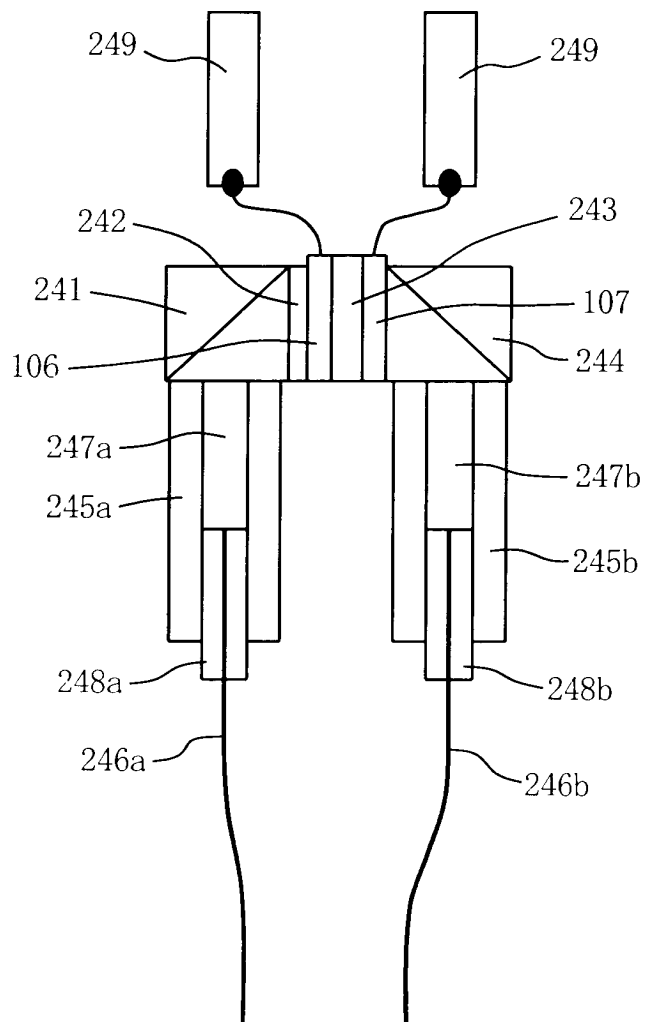


FIG. 31 PRIOR ART

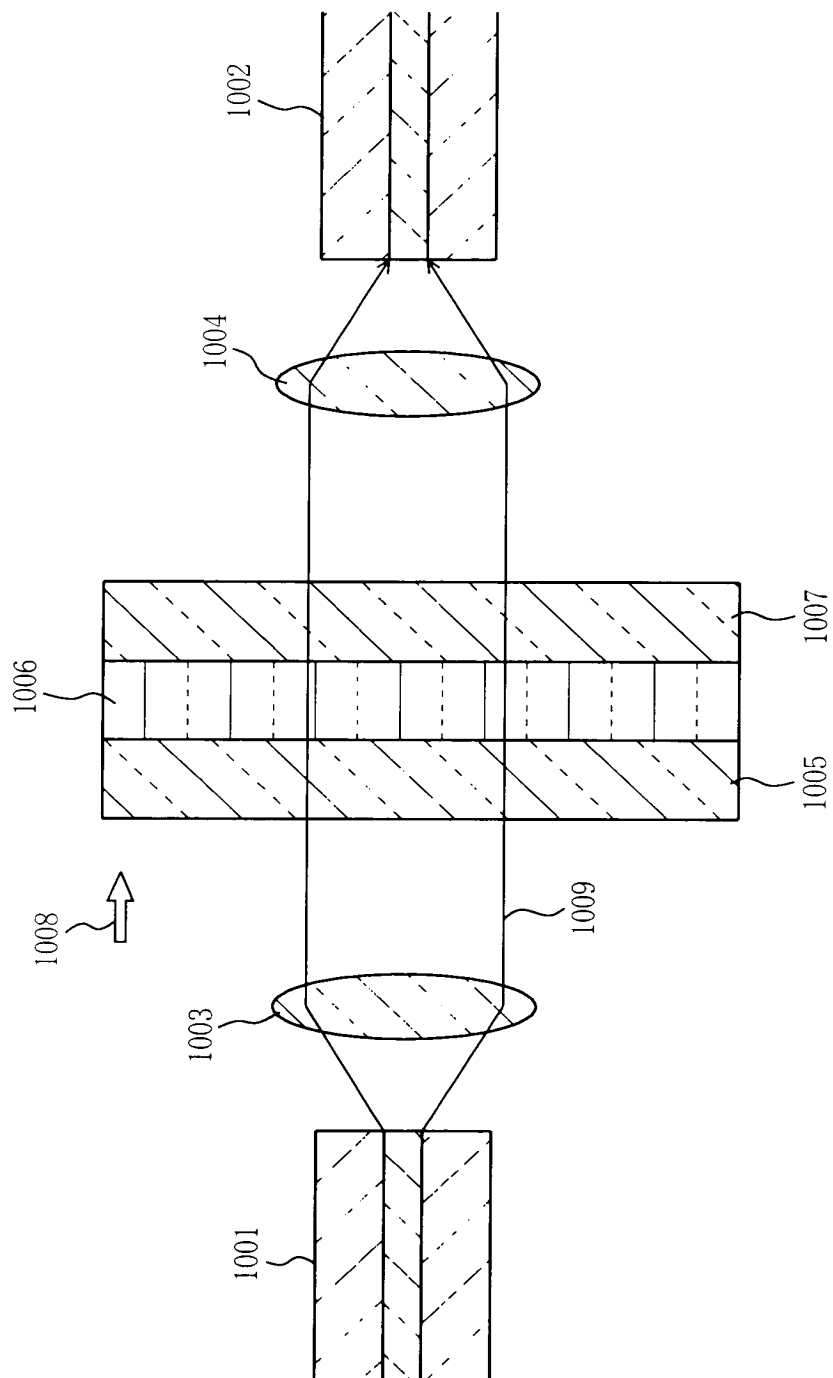
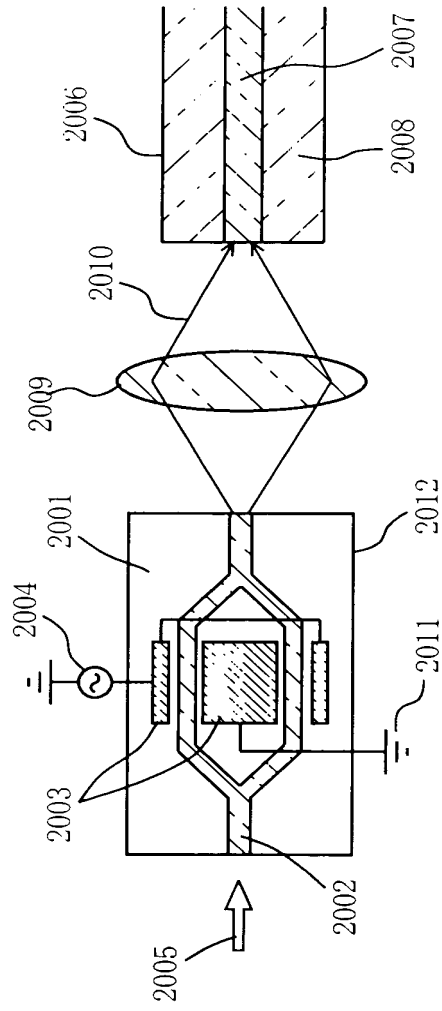


FIG. 32 PRIOR ART



F I G . 3 3 PRIOR ART

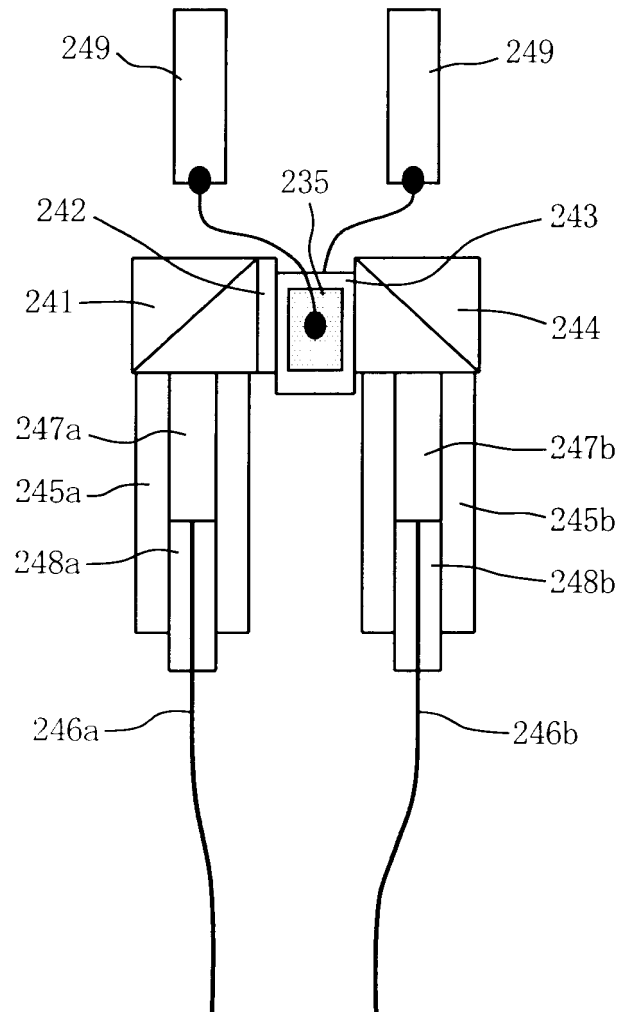




FIG. 34 PRIOR ART

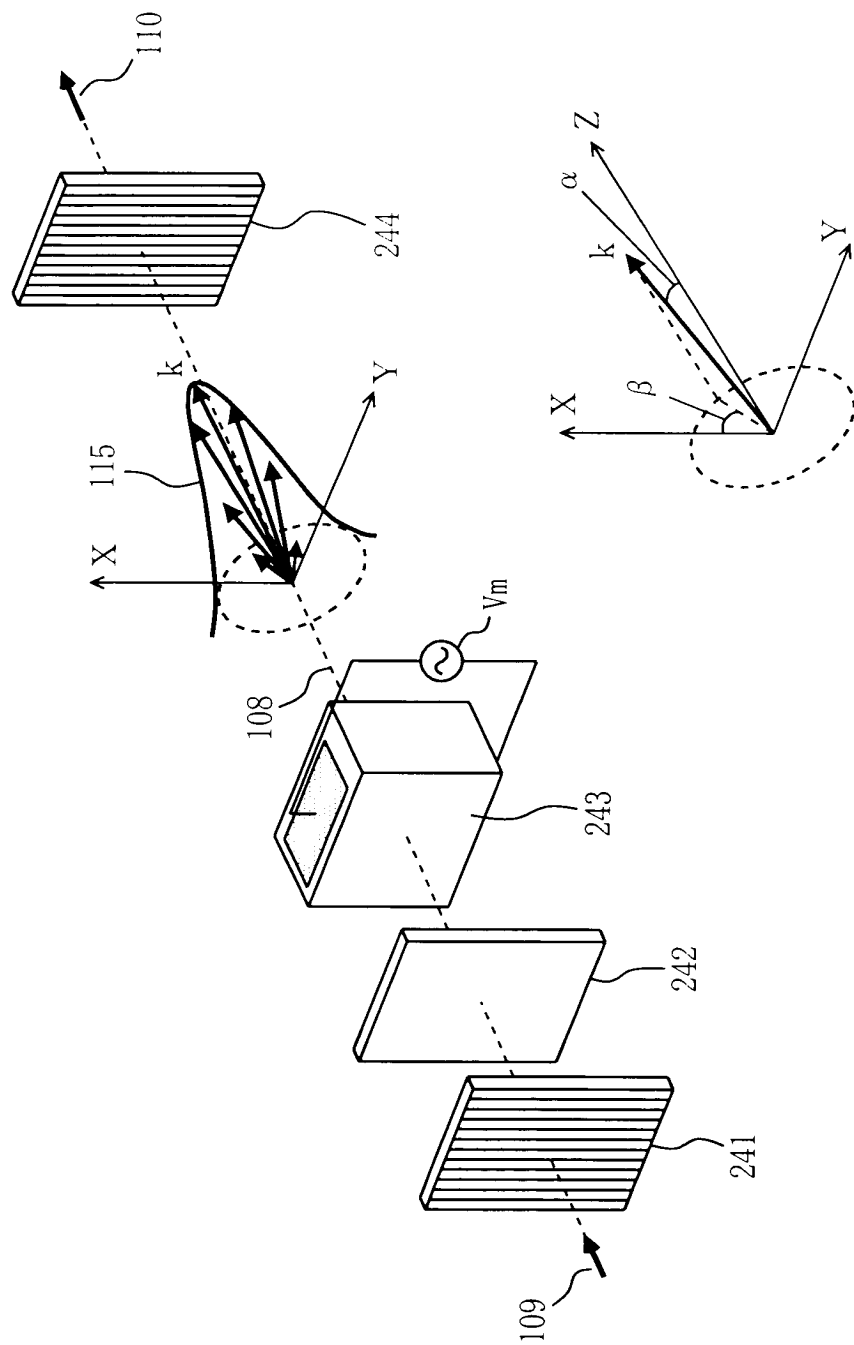


FIG. 35 PRIOR ART

